U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
SCANNED MH 10/1 Q.A. GW	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/880458	D	~~710~~		~~2182~~	V. TAN

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APPLICANTS

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Claimed invention is directed to multiplexing programmable logic clock interconnections with shared pins

TITLE

I/O circuitry shared between processor and programmable logic portions of an integrated circuit

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)
INTERNATIONAL CLASSIFICATION			
			☐ Continued on Issue Slip Inside File Jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to _____ (date) has been disclaimed.	(Assistant Examiner) _____ (Date)			NOTICE OF ALLOWANCE MAILED	
☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____	(Primary Examiner) _____ (Date)			ISSUE FEE	
				Amount Due	Date Paid
☐ The terminal ____months of this patent have been disclaimed.	(Legal Instruments Examiner) _____ (Date)			ISSUE BATCH NUMBER	

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